

Docket No.: TESSERA 3.0-236 DIV
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Beroz et al.

Application No.: Not Yet Assigned

Group Art Unit: N/A

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: ASSEMBLIES FOR TEMPORARILY
CONNECTING MICROELECTRONIC
ELEMENTS FOR TESTING ANDMETHODS
THEREFOR

MS Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each reference was of record in Application No. 09/802,834, the benefit of which is claimed under §120. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: February 12, 2004

Respectfully submitted,

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Substitute for form 1449A/B/PTO				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Masud Beroz
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	TESSERA 3.0-236 DIV

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
AA	US-5,148,266		9/15/92	Khandros et al.	
AB	US-5,915,752		6/29/99	DiStefano et al.	
AC	US-5,518,964		5/21/96	DiStefano et al.	
AD	US-4,455,390		10/3/95	DiStefano et al.	
AE	US-5,798,286		8/25/98	Faraci et al	
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AH	US-5,629,239		5/13/97	DiStefano et al.	
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AK	US-5,148,266		9/15/92	Khandros et al.	
AL	US-5,915,752		6/29/99	DiStefano et al.	
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AO	US-4,818,728		04/1989	Rai et al	
AP	US-6,288,559		09/2001	Bernier et al.	
AQ	US-6,342,443		01/2002	Tao et al.	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
	CA	Multi-Chip Module Technologies and Alternatives; the Basics (Doame and Franzon, eds., 1993, pp. 450-476).			
	CB	Harper, "Electronic Packaging and Interconnection Handbook", McGraw-Hill, Section 5.2, 1991			

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